PHOTONICS ASSEMBLY

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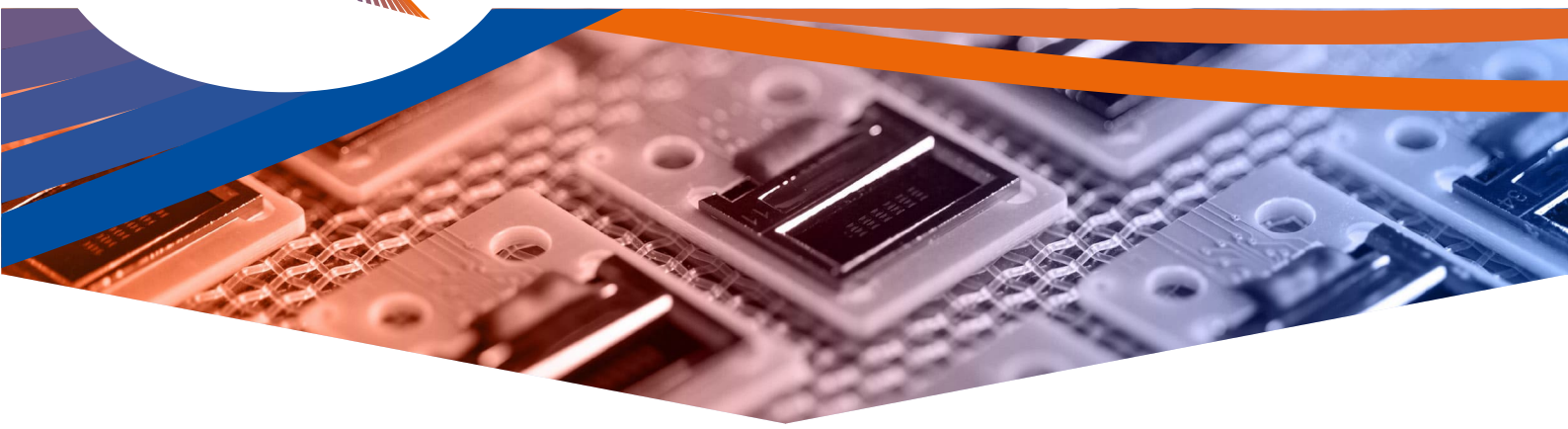

Design Guidelines for Photonic Integrated Circuit Packaging

PHIX is a one-stop-shop for the manufacturing of modules powered by photonic integrated circuits (PICs), from design to volume production. This document describes the core design guidelines for PICs that will enable PHIX to package your PIC into a high performance and cost-effective module that is suitable for a scale-up to volume manufacturing.

1 Validity

This document provides guidelines that are useful for doing the layout of a photonic integrated circuit (PIC) that requires packaging. It demonstrates the best practices for packaging, regardless of the module type chosen for your PIC. Nevertheless, we encourage you to contact PHIX and involve us from the early stages of your PIC design. This allows us to provide tailored advice and to maximize the chance of success of your project. We can then support you with the project planning from tape-out to testable samples.

Please always refer to the latest version of this document. Given the rapid pace of technological advancement, the capabilities and insights in this guide are subject to change.

These guidelines are applicable to all packages and allow the use of standardized assembly processes. Individual design rule documents will become available for our standard packages, outlining module-specific details.

1.1 Version management

v 1.8	January 2025	Modified DC bond pad placing rules

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2 Introduction

Photonic packaging and assembly is a complex and multi-disciplinary design and manufacturing process. To make a PIC-enabled module perform according to specification, sub-micron precision alignment and bonding processes may be required. At the same time, precise thermal management may be necessary to maintain thermomechanical and thermo-optic stability of the signals. The way that the PIC is designed influences many aspects of the packaging process, including:

- The alignment options available to minimize optical losses
- Mode field diameter matching between optical fiber and the chip
- Feasibility and stability of electrical connections through wire bonding
- Radio frequency (RF) signal transmission and radiation
- Mechanical robustness and compactness
- Thermal stability
- Packaging time and cost due to use of custom parts and engineering effort
- Scalability of the module design to higher volume production

...and many more

Many years of experience and collaboration with the PIC designers of our customers around the globe have taught us the benefits of avoiding custom processes and module development. Custom developments are often expensive to set up and do not leverage the power of multiple end users. By using the same standard building blocks as much as possible, we avoid high project risks and financial disappointments of the end user. To this end, we have developed approaches to PIC packaging that:

- Allow PIC designers to enjoy a large amount of freedom in realizing their concepts.
- Limit the amount of non-recurring engineering and customized overhead, so that our packaging services can be cost-effective and provide a quick turn-around.
- De-risk your project and maximize the probability that desired performance will be achieved on the first iteration (from the standpoint of meeting optical alignment and thermal management requirements).

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By following the core PIC design guidelines outlined in this document, you are benefiting from our vast experience in optoelectronic packaging. Your PIC-enabled module will perform at its best, while (start-up) costs and delivery time are minimized. While this applies more strongly to characterization packages and low volume production, these guidelines will also benefit your large volume project and provide a solid route for the scaling process towards it.

Once you have selected a package type, please refer to our relevant Design Rules document for that package, if available. The Design Rules documents build on the guidelines outlined in this document.

3 Supported technology platforms and foundries

PHIX supports all major PIC platforms, such as silicon-on-insulator (SOI), silicon nitride (SiN), indium phosphide (InP), thin film lithium niobate (TFLN), ion exchanged glass, polymer, and other materials with optical functionalities.
We are an independent packaging foundry, so we are happy to work with PICs coming from any foundry in the world.

4 Package solution domains

PHIX can provide packaging solutions for all maturity stages of your technology. Our standard package types, a cross-section of which is listed in section 8, support a wide scope of application domains and manufacturing volumes. In addition, we can support several other industry standard packages, as well as provide custom packaging solutions for higher volume production of your opto-electronic components and devices.

Our characterization packages are convenient for when your PIC is still in the testing phase. These package types provide the optical and electrical interfaces with which you can power and read out your chip without having to probe it. Their open architecture allows for easy visual inspection of the PIC's behavior during its operation, provides relaxed PIC design requirements, and offers high flexibility for customization. An example of such a package type is the PHIX Characterization Package shown in figure 1.

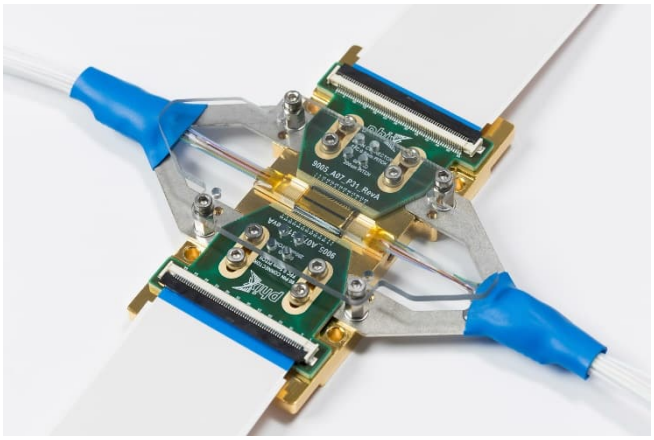

Figure 1: PHIX Characterization Package

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Our offering of various butterfly and large area gold box packages is tailored to applications where the PIC design is more mature, due to their compact and closed architecture. They are suitable when the device around the PIC is in a prototype or demonstrator phase, or when scaling up to small or medium product volumes. Although these package types are robust enough even for high production volumes, it often makes sense to design a custom housing for those products. Please get in touch with PHIX to discuss the possibilities.

Figure 2: Large Area Gold Box package

For higher volume applications our liquid crystal polymer (LCP) overmolded leadframe package can be a good choice. This customizable butterfly or gold box shaped housing is suitable for panel-level assembly. Although limited to only partial hermeticity, the polymer enclosure significantly lowers the cost per unit in medium to high volume production.

5 Intellectual property

Protecting the intellectual property of your company and our own is important to us.
We don't have to know the precise functionality or application of the PIC or module. As long as we are aware of the chip dimensions, electrical and optical interface locations and used mode field diameter, we can package your chip without knowing its function and design details.

For entering into an agreement with PHIX for the packaging of your PIC we have a non-disclosure agreement (NDA) proposal available that protects both our organizations, if you require this.

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6 Introduction to PIC packaging

To help you better understand the reasoning behind our core design guidelines for PICs, we will provide a short description of what a packaging process typically entails. In general terms, the packaging of a PIC involves the following:

- Mechanical package design
- Manufacturing process flow
- Die preparation
- Optical assembly
- Electrical connections
- Thermal management
- Environmental sealing

6.1 Mechanical package design

An early step in the packaging of a PIC is the mechanical design of the envisioned module, which provides constraints for the layout of the chip. Based on the required components within the module, the development stage of the PIC, and the connections to the outside world, it is determined which package is the best fit. Section 8 shows the standard packages currently available at PHIX and provides a link to their specifications.

Apart from the mechanical fit, this design stage determines where mechanical support and/or strain relief is needed and involves an analysis of the required thermal management. A thermo-electric cooler (TEC) and thermistor may need to be placed, or arrangements for passive heat dissipation can be made.

6.2 Manufacturing process flow

In order to assemble a product, a manufacturing process sequence needs to be defined. For some production steps, a small change in the assembly sequence will have a big impact on the manufacturability. For example, the optical alignment of the chip to a fiber array would normally be one of the first steps in the assembly flow. However, due to size constraints of the chip or package, the fiber array may obstruct the wire bond tool and make wire bonding impossible. In that case, the wire bonding will have to be performed before the optical alignment. To reveal any such potential interferences beforehand, we will perform a simulation with virtual tool heads on the mechanical model of the package.

6.3 Die preparation

Depending on your PIC foundry you may receive chips that are singulated and have diced, cleaved, or etched facets. In case you have full wafers, PHIX can perform the singulation step using its wafer dicing processes. The resulting diced PIC facets are typically too rough for low-loss optical coupling to the waveguides, so they require polishing to enhance the surface quality. The dicing process developed by PHIX is optimized such that the polishing time and consumables are greatly reduced due to a reproducible starting point of the process.

Even etched facets may benefit from such polishing steps in order to be able get lower losses between the fiber and chip and to use off-the-shelf standard fiber array configurations.

Many PICs are very thin. This makes them fragile to handle and provides insufficient facet area for the adhesive bonding to other components. For this reason, they are first placed onto a

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submount. This sub carrier may simply increase the effective thickness of the chip, or it may also provide some extra top surface area to make it easier to probe or power it.

6.4 Optical assembly

Examples of optical components that can be interfaced to a PIC are optical fibers or fiber arrays, other photonic chips, and free-space micro-optics like isolators. Alignment of these components is critical to minimize optical losses. During assembly, the thermal and optical properties of the adhesives are also a concern to us. Space also needs to be reserved on the chip design for the adhesive to run out without influencing the chip performance and/or interfering with any consecutive manufacturing process.

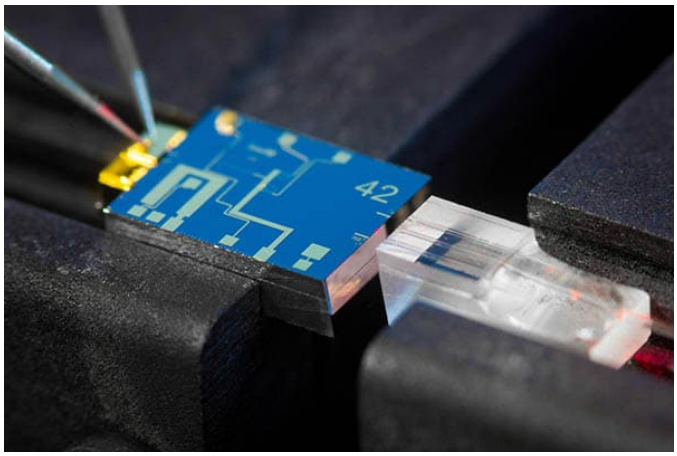

Figure 3: Fiber array alignment to a silicon nitride PIC

Mode field matching between components can also be a challenge. The mode field of optical fibers is often bigger than the required mode field in the waveguides of the PIC. To greatly increase the assembly tolerances and thus produce a more manufacturable device, it is highly recommended to use spot size converters (SSCs) on the chip platform, if they are available.
If tapering to the required fiber mode field is not possible, then an external SSC provided by PHIX can be used.

6.5 Electrical connections

PICs often require electrical connections to a PCB or the module's housing and the most common method for this is wire bonding. In general, wire bonds must be kept short and at a minimal fan-out angle to the chip, to avoid sagging and short-circuiting of the wires. For RF connections, impedance matching, minimal bond line distance, grounding, and minimalization of channel crosstalk are additional challenges.

Within PHIX it is also common to flip chip electronic and photonic components onto the PIC by using thermocompression or soldering processes. However, these are not yet standard processes and require close development with the customer for optimal results.

6.6 Thermal management

Depending on its design and functionality, a PIC may be temperature sensitive, so it is common to include some form of thermal management in a package. A TEC in combination with a thermistor and a control circuit is a common solution for keeping the PIC at the selected temperature.

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Alternatively, passive cooling involves creating a path of low thermal resistance between the PIC and the housing. With this solution, the PIC's temperature follows that of the housing.

6.7 Environmental sealing

For prototype packages an open enclosure is often useful to allow for visual inspection and debugging of the PIC during its operation.
For most industrial packages the chip is typically closed off non-hermetically inside the module. The addition of desiccant materials can help enhance the lifetime of the module.
For more demanding applications, PHIX offers hermetically sealed housings with a gas (such as nitrogen) or a vacuum inside. Hermetic gold boxes have become a standard in the telecommunications industry, but much more cost-effective electronics packaging methods may be sufficient for your PIC's application. Recent great advancements in the area of chip passivation also makes hermetic sealing unnecessary for a range of new applications.

7 PIC Design Guidelines for Packaging

At a high level, the assembly approach used at PHIX is based on the following best practices:

- Allocation of chip edges by optical or electrical function
- The use of alignment loops for active optical alignment and basic process control
- Taking into account mode field matching
- Considering clearances for adhesives and tooling
- Placing bond pads with wire bond feasibility in mind

7.1 Allocation of chip edges

When viewing the PIC from the top, its edges can be defined by the designations north, south, east, and west. As indicated in figure 4, if two edges are required for optical connectivity, we strongly recommend allocating the east and west edges to this, and the north and south edges to electrical interfaces. This distinction is made to enable mechanical clamping on the north and south sides during die polishing and optical assembly, without other optical interfaces getting in the way or polished surfaces getting damaged.

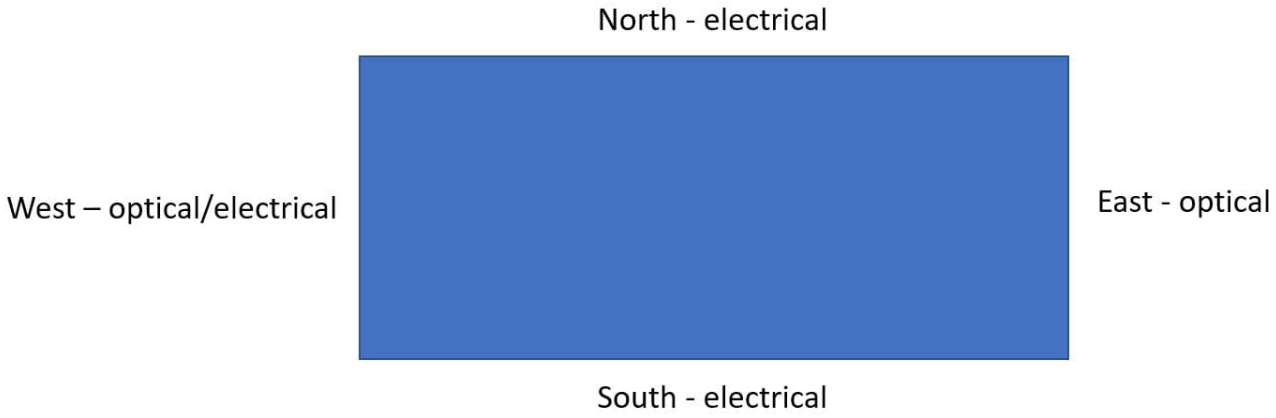

Figure 4: Chip edge allocation on a PIC (top view)

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7.2 Fiducial markers

To facilitate the (automated) PIC packaging process PHIX recommends the placement of fiducial markers on the chip. To help you place them in your design we provide a sample GDS file, which can be requested from PHIX. There are two types of markers, as indicated in figure 5:

- Chip orientation markers
- Polishing rulers

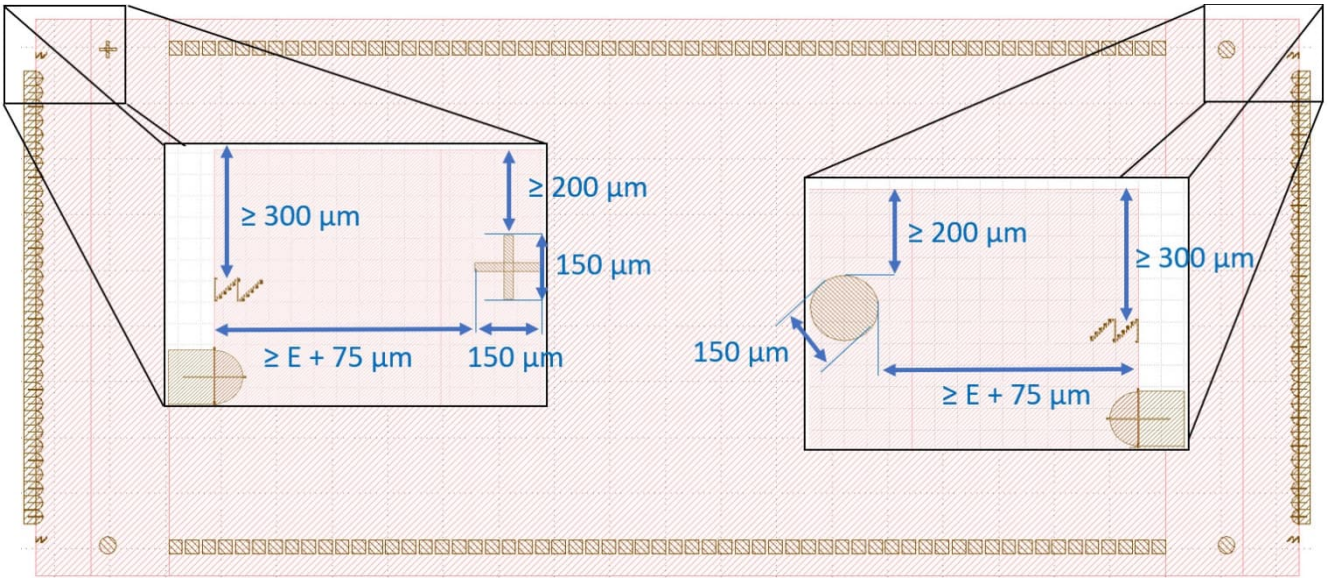

Figure 5: Overview of fiducial markings for PHIX

7.2.1 Chip orientation markers

The chip orientation markers help us identify the facets of the PIC and are used by some of our machines to perform automated alignment. They consist of an equal-armed cross in the northwest corner and circles in the other corners, in the oxide and metal layers of the PIC. We recommend the cross to have arms of 150 µm and the circles to have a diameter of 150 µm. These markers should be kept 200 µm from the electrical facets and E + 75 µm from the optical facets, where E is the clearance distance for adhesives. The value of E is different for an edge coupling or grating coupling configuration, respectively 500 µm and 1250 µm (see section 7.9 for more details).

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7.2.2 Polishing rulers

Polishing rulers are used as markers for polishing of the optical facets. We require two of these rulers per optical facet, positioned at least 300 µm from the chip corners in the waveguide layer. We recommend a ruler with a 5 µm division that goes from 0 to -100 µm. The optimum fiber core coupling point should be positioned in the range of 0 to -30 µm. The ruler must be aligned to the chip edge depending on the specific foundry design rules.

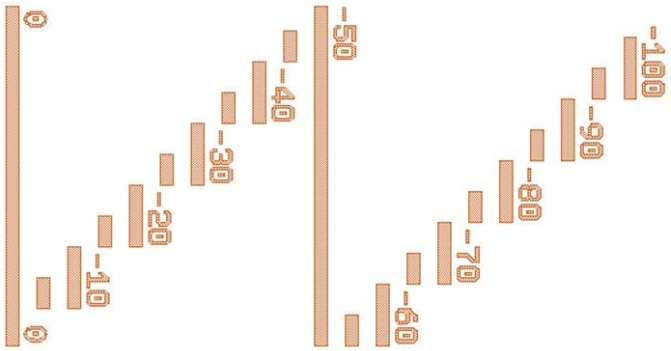

Figure 6: Polishing ruler details

7.3 Dicing and polishing

7.3.1 PIC states before packaging

There are five states in which PICs can reach PHIX at the start of the packaging process:

1. On a wafer, with no dicing or etching whatsoever. PHIX will perform the dicing.
2. Diced or cleaved by the PIC foundry.
3. Etched all the way through at the optical interfaces.
4. With a deep trench at the optical interfaces to expose the waveguides and inverted taper.
5. With a deep trench and suspended edge couplers.

7.3.2 Deep trench with inverted taper for SiPh edge couplers (state 4)

If a deep trench is combined with an inverted waveguide taper at the optical interface of a SiPh PIC, then PHIX has a special instruction that will allow us to polish the optical facet without compromising the taper.

PHIX requires a waveguide section of fixed size and constant target mode field diameter (MFD), located before the start of the actual taper. This waveguide section should be at least 30 µm long, corresponding to the polishing landing area (between 0 and -30 µm, see section 7.2.2). Our polishing process will remove material to get as close as possible to the -30 µm marker, but not go beyond.

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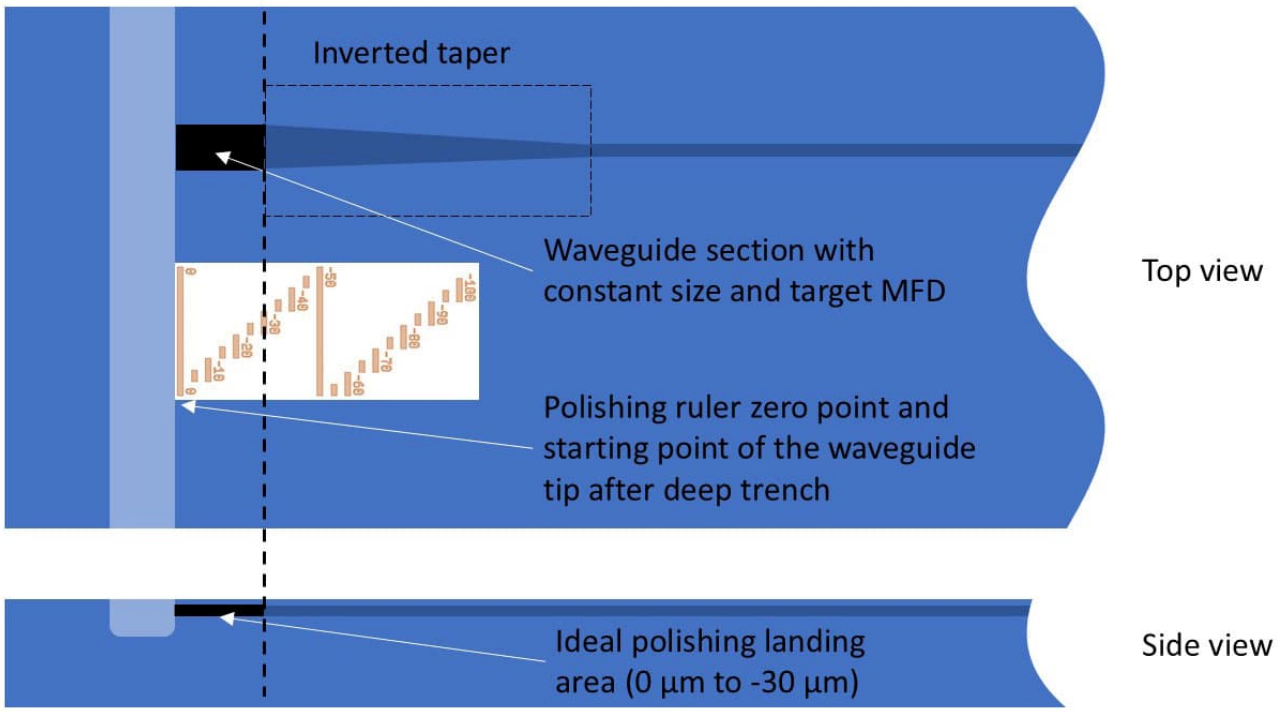

Figure 7: Extended waveguide after inverted taper

7.3.3 Deep trench with suspended taper for SiPh edge couplers (state 5)

Silicon photonics (SiPh) foundries can create suspended edge couplers by adding a fabrication step that etches away a portion of material under the SiO_2 layer. This allows foundries to better confine the waveguide mode and enlarge its mode field diameter (MFD), typically up to 9 x 6 μm^2. In principle, this enables lower coupling losses to standard single mode fiber (SMF) compared to, for example, an inverted taper. A 3D representation of the suspended edge coupler can be seen in the picture below.

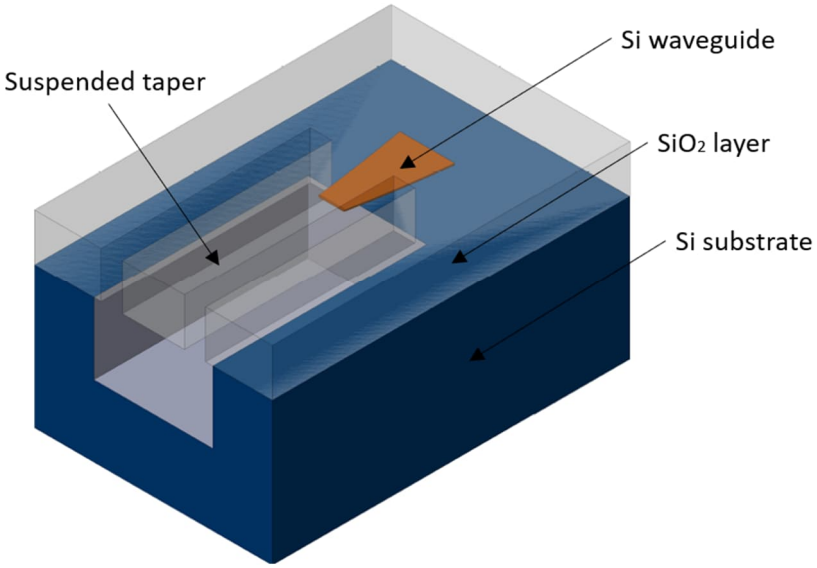

Figure 8: 3D representation of a suspended edge coupler

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Foundries have slightly different ways of processing these suspended edge couplers, which may affect the packaging choices. Involving the foundry and PHIX in the PIC design is in this case highly recommended.

The nature of this suspended structure, especially its fragility, adds new challenges to the packaging. PHIX offers two alternative methods that enable safe coupling to these suspended edge couplers.

The first method is an assembly process developed by PHIX that involves a glass lid being placed on top of the PIC and its suspended waveguides. This lid, attached with low-refractive-index epoxy, allows PHIX to safely polish and assemble the PIC with suspended tapers. To enable the placement of this lid, a keep-out area in the proximity of the waveguides needs to be reserved. A rough estimate of the required keep-out area is described in figure 9 below. Please do not place structures on the chip within this area that may not function properly if covered with epoxy. Depending on the PIC size this may also affect the clearance from the PIC edge to the first bond pad, increasing this value for standard edge coupling configurations from 1200 µm (see section 7.9) to 2500 µm.

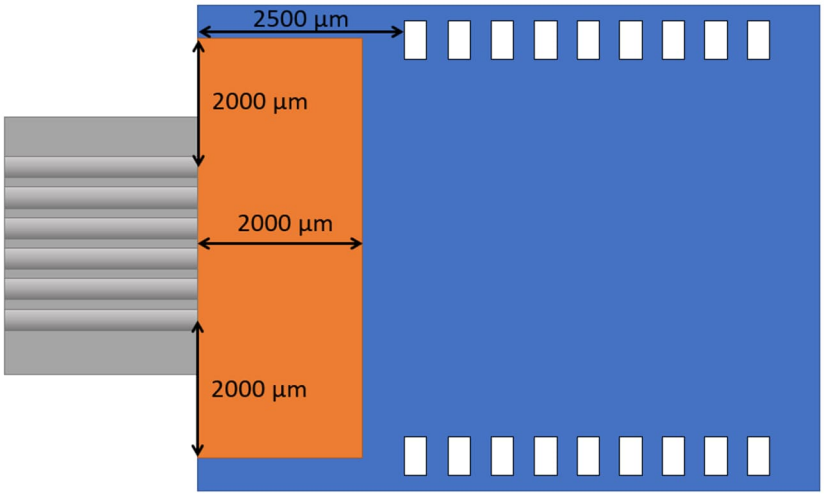

Figure 9: Waveguide keep-out zone in case of glass lid placement

The second method involves attaching the PIC with suspended SiPh edge couplers directly to a fiber array without a polishing step. In this case, the fiber array will be assembled directly to the etched step and a physical gap will remain between the waveguides and the fiber cores. This gap is filled with low-refractive-index epoxy and results in a small coupling loss due to the large MFDs at play. As a downside, this optical joint is typically less strong than a regular fiber array attachment, and requires consideration during the package design. For example, it may require an additional strain relief method between the fiber array and the mechanical base, in order to better maintain the alignment. A sketch of this second optical assembly method of a PIC with suspended SiPh edge couplers is visible in figure 10 below.

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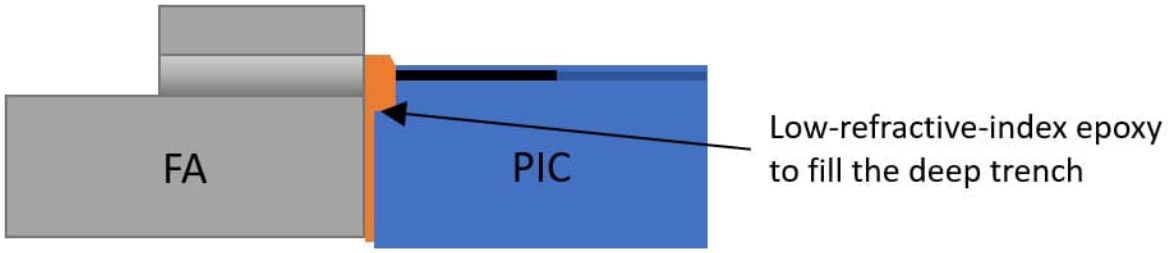

Figure 10: Direct fiber array attachment with a physical gap

The suspended edge coupler waveguide technology is rather new and the selection of the method of how to deal with this should be discussed with PHIX in detail during the PIC design phase.

Retracted lid fiber array assembly is currently not offered by PHIX.

7.4 Fiber coupling

Fiber arrays can be coupled to PICs in three different ways, by edge coupling or by two variations of grating coupling. This is illustrated in figure 11 below.

Edge coupling is preferred since it provides the lowest insertion loss, is compatible with a wide range of bandwidths, and has a low sensitivity to polarization. Optical alignment in this scheme is challenging, but the strategies and processes of PHIX, as outlined in the section below, provide great coupling accuracy.

Grating coupling offers more relaxed alignment tolerances for coupling light to and from the PIC, at the expense of insertion loss performance, bandwidth range and polarization sensitivity. Traditionally, the near-vertical orientation of the fiber array provides a bulky and fragile packaging solution, suitable only for prototyping. However, a quasi-planar approach to grating coupling, using a 40° polished facet with total internal reflection, allows the fiber array to lie flat on the PIC (figure 11c). This provides a much more compact and robust configuration.

Our fiber arrays have standard pitches of 127 or 250 µm. Whatever coupling scheme is used, the waveguide pitches should match this.

Some of our standard package types support fiber arrays of up to 64 channels. Please refer to our standard package type specifications for maximum channel counts.

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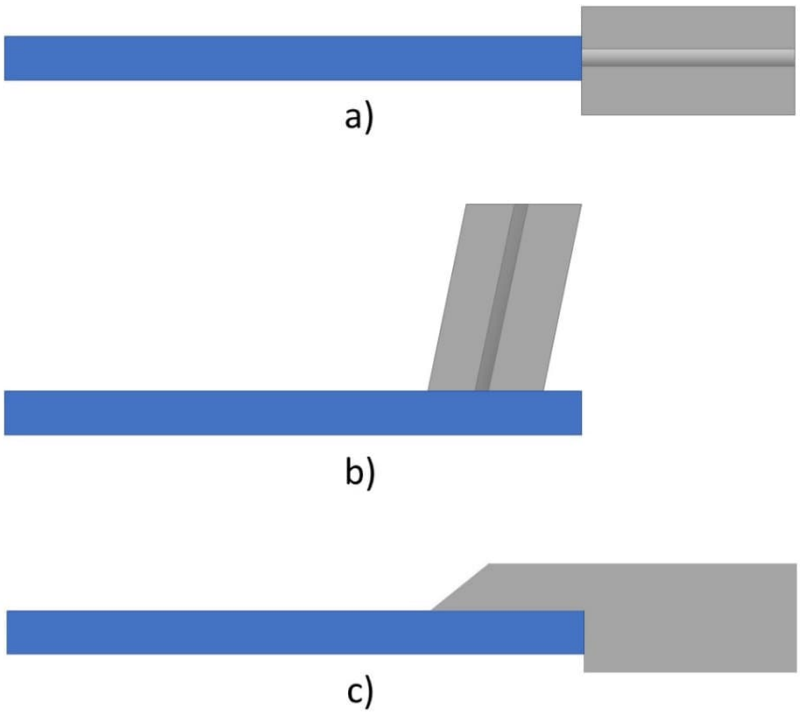

Figure 11: Fiber coupling schemes: a) edge coupling, b) vertical grating coupling, c) quasi-planar grating coupling

7.5 Alignment Loops

When a fiber (array) or another optical chip is to be bonded to a PIC, alignment is critical. The most accurate and reproducible positioning process is active alignment. Active alignment is the method where light is shone through the waveguides of the components and the position with the lowest optical losses is recorded.

While some chips have light sources in the circuitry that can be used for this process, this requires active probing of the chip with custom probes. However, since the output signal of such a gain element is not calibrated, no absolute performance figure can be derived.

To address this challenge, PHIX recommends one set of waveguide alignment loops (also referred to as optical shunts) for each optical interface.

The requirement of the extra fibers for this active alignment strategy raises the cost of the module, but greatly reduces the level of customization. This allows multiple customers to transition to automatic alignment equipment through their scale-up phase. When the volumes increase, we will work with you to define the best strategy to reduce the cost of the module without compromising its manufacturability.

Furthermore, if these alignment loops are made of unequal length, we can measure the interface loss and the waveguide loss separately. This data about the alignment accuracy achieved by PHIX and your chip's waveguide loss provides valuable statistics for the scale-up phase of your project.

Figure 12 below illustrates this approach based on the example of a main chip PIC1 with both a fiber array (west) and another chip PIC2 (east) coupled to it. The fiber array has an extra eight

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fibers allocated to the alignment loops. The two inner sets of loops are used for aligning PIC1 to the fiber array and the two outer sets are allocated to waveguides for aligning PIC2 to PIC1. With our in-house automated equipment, we can use a temporary fiber array which we align to PIC1 using the alignment loops. Next, we can align PIC2 to PIC1 using the other set of alignment loops by reading out the temporary fiber array and we bond the chip into place. Then the temporary fiber array can be replaced with a smaller configuration only spanning the alignment loops of PIC1.

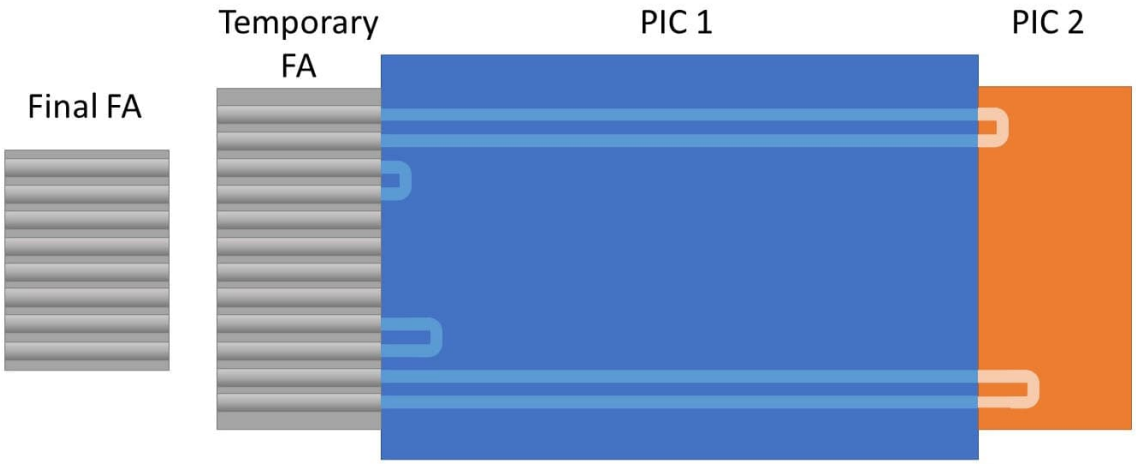

Figure 12: Example alignment loop configuration of two PICs and temporary and final fiber arrays (FA)

It is beneficial if each of the two loops are separated by as much distance as possible. During the alignment process, the optimal alignment position for each loop is detected. In figure 12, the outermost channels of each of the components is chosen to maximize the distance between the loops, and some minor waveguide routing is done on PIC 1 to facilitate this.
Note that it is not necessary to have a large separation between the input and output couplers within each individual loop.
Alignment of grating coupled fiber arrays involves fewer degrees of freedom and the tolerances are a little more relaxed. For this reason, it is also possible to work with a single alignment loop, as pictured in figure 13.

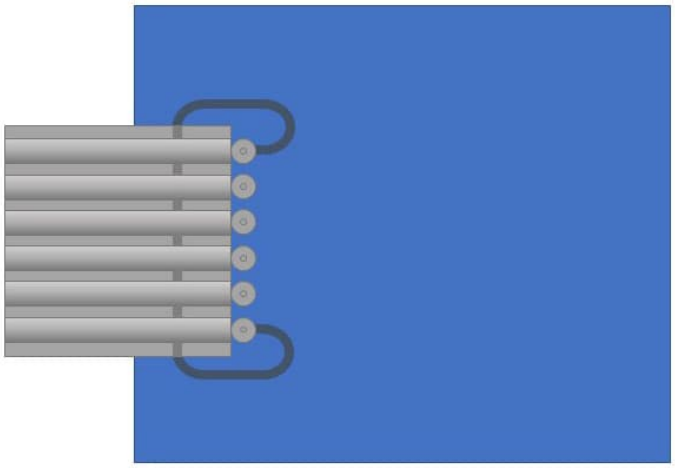

Figure 13: Single alignment loop for grating coupled fiber array

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7.6 Multiple optical components on one edge

At PHIX it is possible to bond more than one optical component to the (east or west) edge of the PIC. However, there are clearances that must be allowed in order to enable the gripping of the components during bonding. Therefore, each device along the same edge must be spaced at least 4 mm apart. Be aware that the distance between the optical interfaces on the chip may need to be larger.

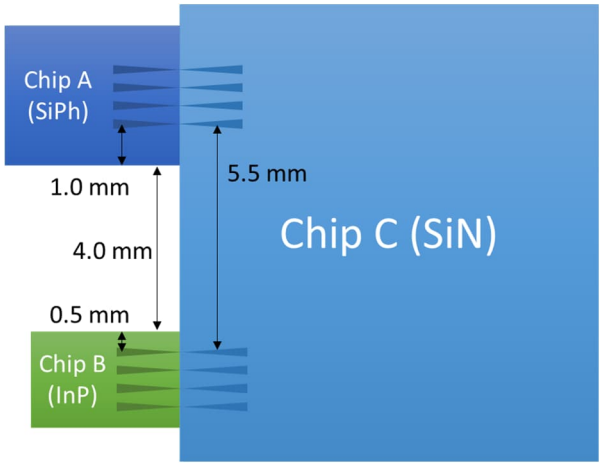

Figure 14: Required clearance between two chips bonded to the west facet of the PIC

The example in figure 14 of a heterogenous hybrid assembly illustrates what this means for the required spacing on the PIC (Chip C).
If Chip A has 1 mm shoulder between its edge and its southernmost interconnect, and Chip B has 0.5 mm shoulder from edge to northernmost interconnect, then the spacing between the last and first couplers of their interconnect banks on the PIC (Chip C) must be at least 5.5 mm.
Do not forget to take into account the extra waveguides used as alignment loops, as specified in section 7.5.

7.7 Fiber types and mode field matching solutions

7.7.1 Optical fiber types, power limit, and mode field mismatch

PHIX offers PIC to fiber packaging solutions for a broad wavelength range, spanning from the visible spectrum up to the near infrared. We can couple arrays of many different optical fibers, be it single mode, polarization maintaining or specialty fiber. Table 1 lists a few of the most used fibers in the telecom band.

	Wavelength (nm)		Fiber type	MFD (µm, ± 0.5 µm)	
	Min	Max		@ 1310 nm	@ 1550 nm
SMF28	1270	1625	SM	9.2	10.4
PM1310	1260	1360	PM	9.0	n/a
PM1550	1500	1600	PM	n/a	10.5

Table 1: Wavelengths and mode field diameters of common fiber types

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The optical interface power limit per channel is 20 dBm (100 mW) at 1550 nm with a 10 µm mode field diameter (MFD). A higher optical power, lower wavelength, and/or smaller MFD may degrade the index-matching epoxy present at the optical interface between fiber array and PIC.

If your wavelength is outside the telecom band, specifications like MFD, power density, and reliability require careful consideration. Do not hesitate to contact PHIX for guidance when operating in wavelength ranges outside the telecom band, especially the visible range.

When edge coupling optical fibers to a PIC, there may be a mode field mismatch that needs to be dealt with in order to minimize insertion losses. For example, the MFD of 1550 nm wavelength SMF28 single mode fiber is typically 10.4 µm, whereas in a PIC waveguide it may be as low as 1.5 µm. There are several possible solutions to deal with this mismatch.

7.7.2 On-chip spot size converters

As the most preferred solution for mode field mismatches between the optical fiber of your choice and your PIC, PHIX recommends using a lithographically defined on-chip spot size converter. If your PIC technology has such a building block, this is highly recommended. Even if you cannot expand to the full fiber mode field diameter, having the largest possible mode field on the chip will help to obtain more relaxed alignment tolerances and therefore improved manufacturability.

7.7.3 PHIX spot size converters

As an alternative or a supplement to on-chip spot size converters (SSCs), PHIX offers off-chip SSCs that are attached to the fiber array, as shown in figure 15. Depending on the required mode field, these optical interposers are made of ion-exchanged glass or silicon nitride and can be interfaced to PICs of any common material. A variety of standard mode fields (both circular and elliptical), pitches, and channel counts are available off-the-shelf, supporting both single mode and polarization maintaining connections.

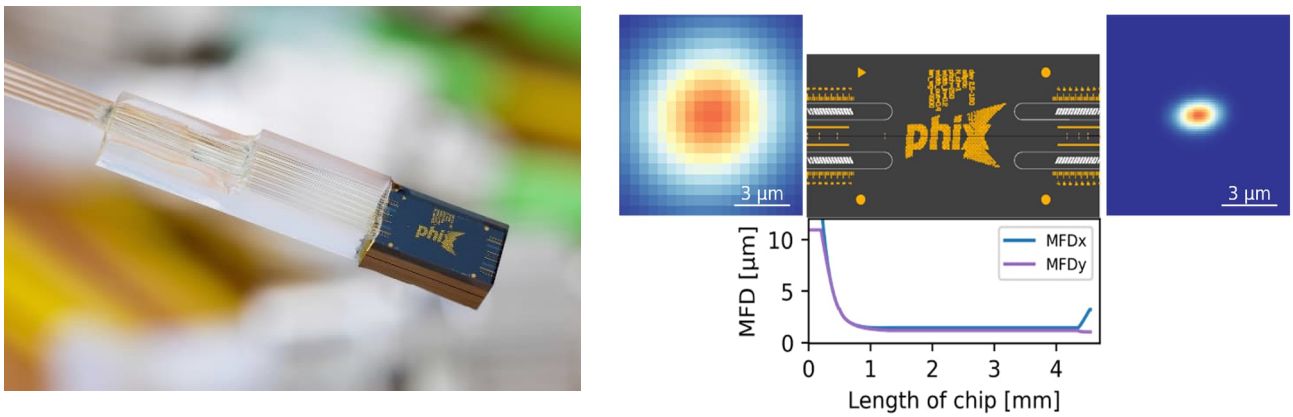

Figure 15: Off-chip mode field reduction using a fiber array with attached spot size converter

These SSCs are lithographically defined and will provide more repeatable and reproduceable coupling when compared to other mode field conversion methods, especially in situations with high channel counts (> 12 channels) and small MFDs (< 3 µm).

The PHIX SSC offering is in continuous development. Some recent advancements have been:

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- Producing SSCs with angled waveguides and elliptical modes, especially interesting for InP PIC interfacing.
- Development of SSCs for high density interconnects suitable for reduced-cladding fiber types at a pitch of 84 µm, especially interesting when space becomes a constraint at the system level.
- Exploration of the O-band with MFD conversion from 10 µm to 3 µm and channel counts between 16 and 64.

For available SSCs please check the PHIX website or contact our sales department at sales@phix.com.

7.7.4 Ultra-high numerical aperture fibers

As an alternative to the use of PHIX SSCs, mode field matching is also possible using ultra-high numerical aperture (UHNA) fibers. These are mainly used in the telecom band (1100 to 1600 nm) and are supported by PHIX as a custom option.
UHNA fiber arrays are manufactured by splicing short pieces of UHNA fiber to regular fibers inside the v-grooves of the array, resulting in a reduced MFD at the interface without increasing the size of the package. A typical MFD that can be reached with UHNA fiber lies between 3.2 and 4.8 µm.

Not all UHNA fibers can support a polarization maintaining requirement, so this may further limit the available options in terms of MFDs.

As UHNA fiber arrays combine inherent positioning inaccuracies of the fibers inside the v-grooves with small MFDs at the interface, a lower and less repeatable coupling performance may result when compared to the lithographically defined waveguides of the PHIX SSCs. The choice between a PHIX SSC and a UHNA fiber array is often a tradeoff between performance, cost, and scalability. As a general rule of thumb, a UHNA fiber array can work well up to a channel count of 12 to 16 fibers. Above this channel count we often advise an external SSC. PHIX is happy to help you make the best tradeoff for your application.

7.8 Angled waveguides

If back reflections at the chip facets are a concern, the use of angled waveguides can be considered. These can either be realized by angular positioning or angular polishing.

Angular positioning places the waveguides at an angle to the chip's facets in the x-y (length/width) plane (see figure 16). This approach is very suitable when edge coupling two photonic chips together. Angular positioning is not recommended for edge coupling to fiber arrays, because polishing a fiber array in this plane creates a high margin of error for the effective pitch between the fibers, which potentially increases the insertion losses. An exception is when PIC 1 is indium phosphide, where angular positioning is the norm because angular polishing (see below) is not possible for this material.

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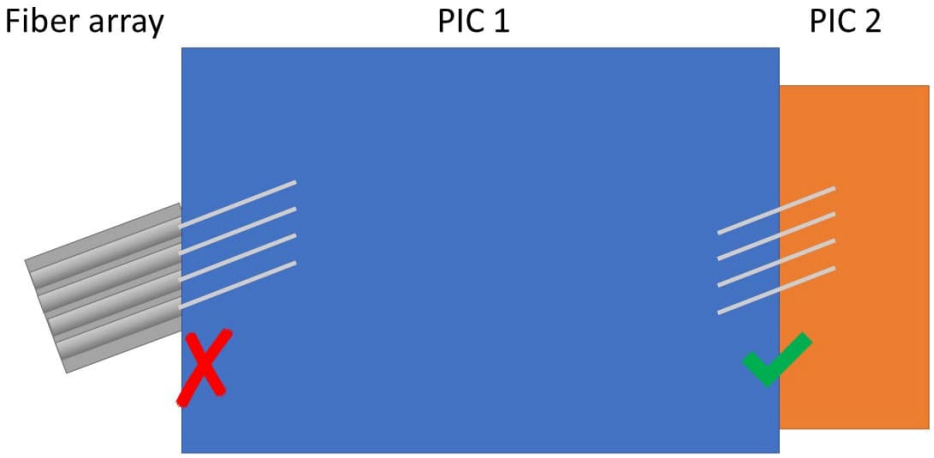

Figure 16: Angular positioning of waveguides

PHIX can perform angular polishing, creating angled facets in the z (thickness) plane (see intersection of figure 17). The waveguides stay at right angles to the chip facets when viewed from the top. This method is very suitable for edge-coupling fiber arrays to PICs where the contrast is low and angles of 8 degrees are sufficient for diminishing the reflections. It is not recommended for chip-to-chip coupling, particularly if one of the platforms is indium phosphide.

Figure 17: Angular polishing of the fiber-to-chip interface

If the thickness if your bare die is lower than 0.7 mm, PHIX will typically place a submount underneath it in order to provide mechanical support during the polishing process.

7.9 Clearances for adhesives

When bonding optical components such as fiber arrays to the PIC, either by edge coupling or grating coupling, the adhesive will form fillets. This means that there will be some overrun of the adhesive onto the chip. To avoid the adhesive covering bond pads or other sensitive areas on the chip surface, clearances need to be considered. There will be a necessary exclusion zone around the edges and the chip surface where the optical interconnections are made. In addition, the bond pads on the north/south edges should be no closer than 1500 µm to the east/west edges for grating coupling and 1200 µm for edge coupling.

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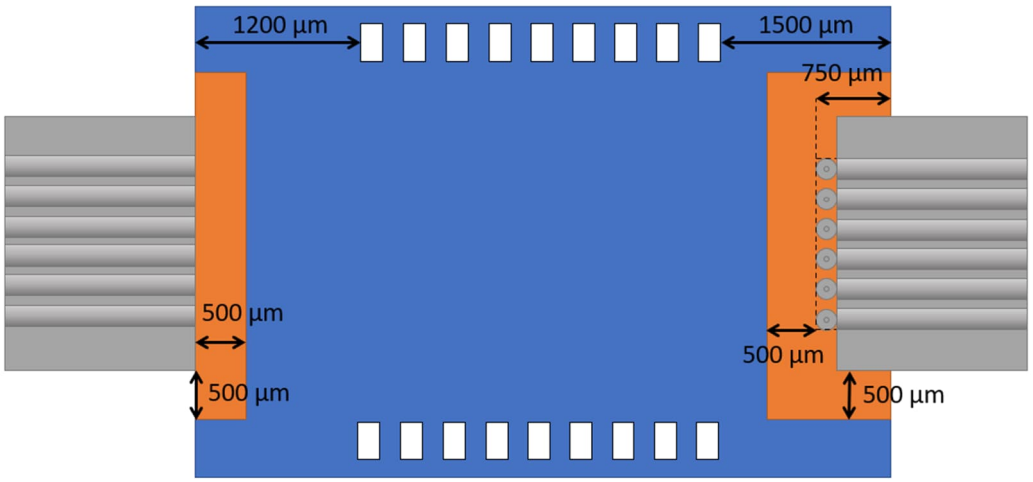

Figure 18: Space reserved for adhesive fillets in an edge coupling (left) and grating coupling (right) configuration

7.10 Wire bonding considerations

Wire bonding provides the electrical connections within the package between PICs, PCBs and the housing. Our standard is to use 17.5 µm gold bond wire to perform wedge-wedge bonding. In general, wire bond lengths should be minimized to reduce the risk of sagging and short-circuiting of the wires. Bond pads can be placed at the north and/or south edges of the PIC, as explained in section 7.1. They should have a gold (Au) or aluminum (Al) surface finish. Please take care to avoid oxidation of Al surface finishes due to aging or improper storage of the dies, as this may create adhesion issues during the wire bonding process.

7.10.1 Tooling clearances

In the case of fiber arrays and edge coupling, the lid of the fiber array unit juts above the level of the top surface of the chip. In the case of grating coupling, in a vertical or quasi-planar configuration, the fiber array extends vertically from the surface of the chip, and is best segregated to as close to an edge as possible. In each of the coupling schemes, the fiber array unit can cause obstruction during wire bonding.

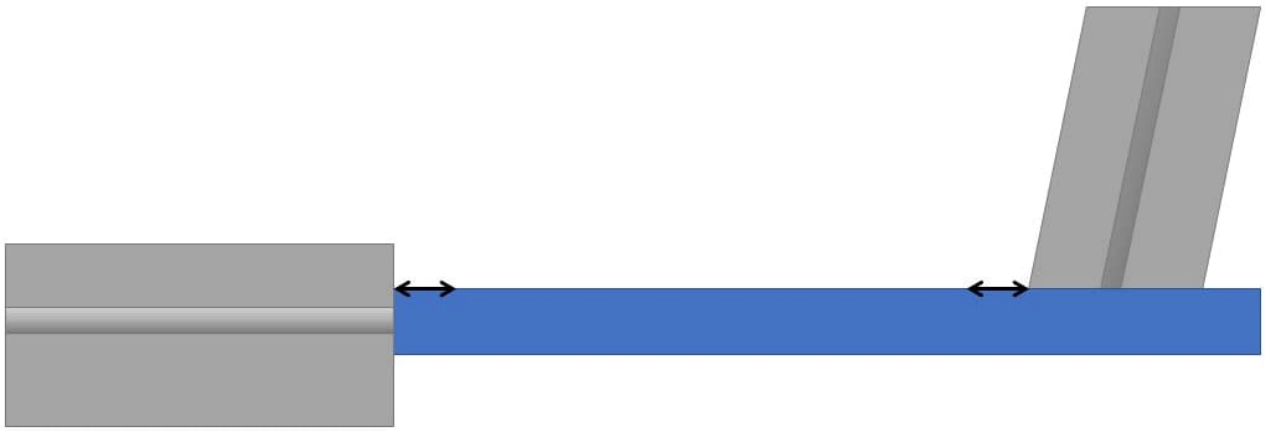

Figure 19: Tooling clearances required on the PIC (side view) for edge coupling (west) and grating coupling (east)

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When it is time for wire bonding, there needs to be sufficient clearance in all dimensions around the pads for the wire bonding capillary. The generic design rules for pads provided below are intended to ensure this clearance, but a 3D mechanical check with a model of the capillary to be used is also performed by PHIX engineers to validate customer-specific designs.

7.10.2 DC bond pad size and pitch

We recommend square or rectangular bond pads with a shortest edge of at least 90 µm in length. The bond pad pitch should be at least 150 µm to ensure that standard PCB technology can be used. If your application demands a higher bond pad density then we have several custom options available. Please contact PHIX to select the best method for you.

7.10.3 DC bond pad placement

With regard to the placement of bond pads, the following guidelines are applicable:

- Observe the clearances for adhesives covered in section 7.9 to keep the bond pads clear of the optical facets of the chip.
- The distance between a bond pad and the edge of the PIC should be greater than 100 µm. This ensures that bond pads are safe during wafer dicing. The maximum distance is 500 µm. This prevents wire bonds to be too long and at risk of sagging. If PHIX is required to perform the wafer dicing, please discuss the dicing plan and details with our team.
- We recommend a bond pad width and length of 120 µm ± 30 µm and a pitch of 200 µm ± 50 µm.
- Just a single row of bond pads on the north and south side is suggested. Using staggering rows of bond pads on the PIC to save space greatly complicates the assembly.

These guidelines are illustrated in the figure below.

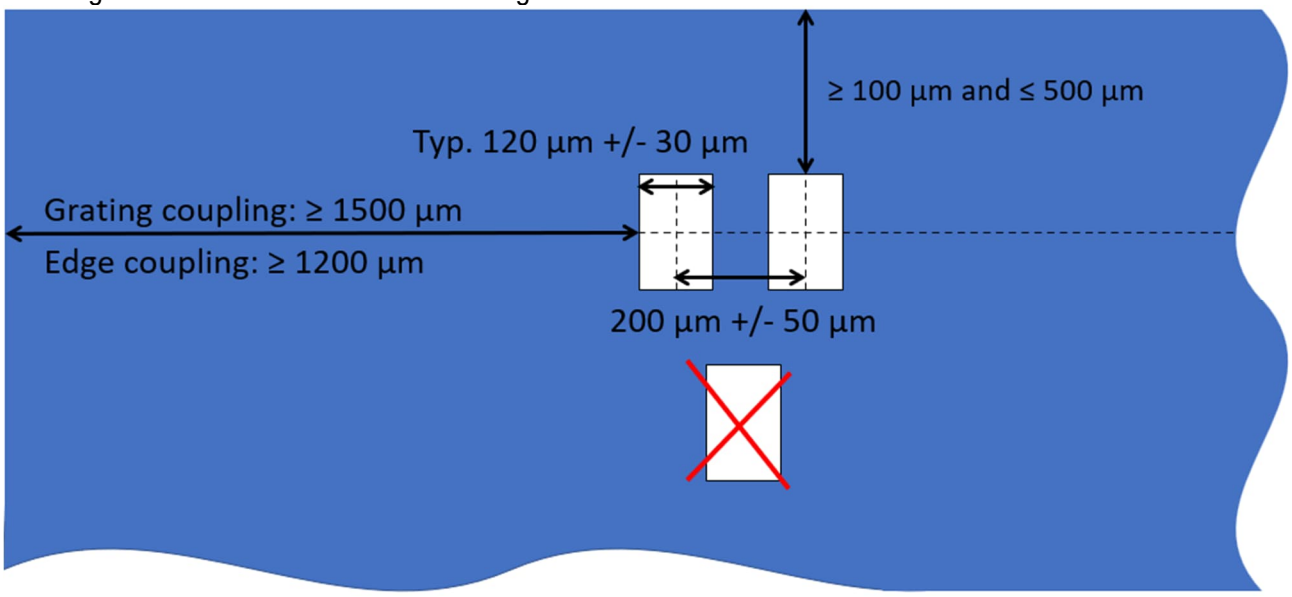

Figure 20: Bond pad placement rules

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7.11 RF electrical interfacing

PHIX supports RF electrical interfacing with frequencies from the kHz range into the tens of GHz. Depending on your exact needs, this poses additional challenges related to impedance matching and minimalization of parasitic losses. Because the optimalization of the performance of the RF interface involves many parameters, on both the PIC and the PCB, the most important guideline we would like to give is to involve PHIX early in the design process.

When designing the RF electrical interface for your PIC, we have three main objectives.

1. Minimize signal reflections and losses to an acceptable level
2. Match the characteristic impedances on the PIC side and PCB side
3. Confirm that wire or ribbon bonding is feasible and these connections can be made as short as possible to maximize the RF performance.

In the following sections we will explain how these objectives lead to guidelines relating to the sizing and placement of bond pads and why it is beneficial that we work together already at the PIC design stage to optimize your chip for packaging.

7.11.1 RF bond alignment

In order to avoid impedance reflections in RF signals, wire or ribbon bonds between your PIC and our PCB should be of minimal length and provide a smooth transition. This is one reason why we aim to align the bonds pads of our PCB as closely as possible with those on the PIC, creating a straight bridge.

Another reason is that a close alignment means that bonds can be as parallel as possible. Parallel bonds avoid the risk that the tails of the wedge bonds accidentally touch each other and create shorts.

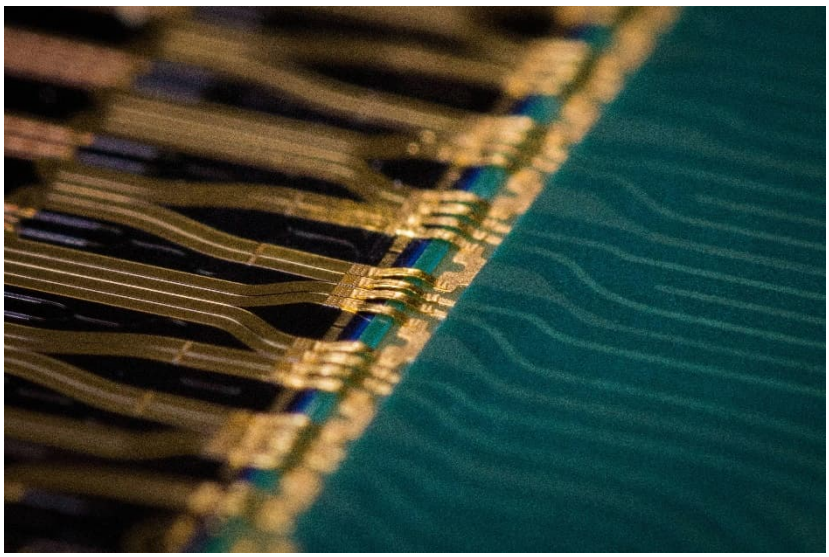

Figure 21: Aligned ribbon wire bonds between PIC and PCB

7.11.2 Impedance matching

As impedance mismatch can lead to signal reflection and inefficient power transfer, we aim to match the characteristic impedances of the PIC and the trace line on the PCB or ceramic as closely

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as possible. The characteristic impedance of each side of the interface depends on four parameters.

- The width *w* of the signal trace S
- The clearance *x* between the signal trace S and ground traces G
- The thickness (depth) *z* of the signal trace S
- The dielectric constant κ of the material

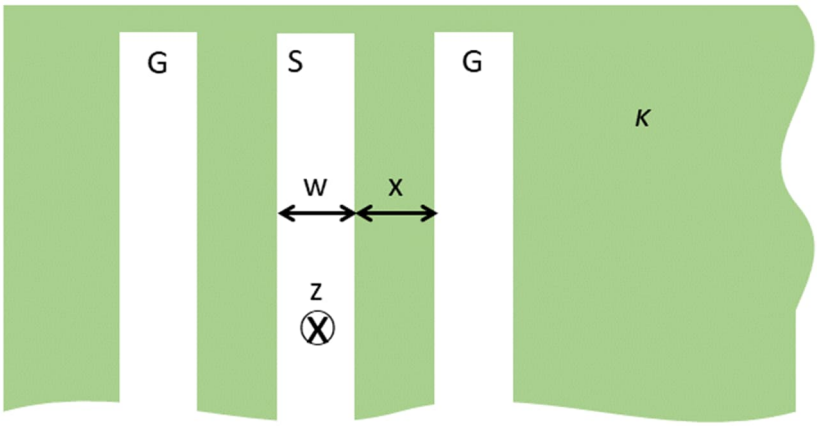

Figure 22: Parameters influencing characteristic impedance for single-ended traces

Our goal of minimizing wire bond lengths and making them as parallel as possible means that we aim to closely match the first two parameters between the PIC and the trace line. However, the dielectric constants between the PIC and trace line materials may differ significantly, and there is often limited room to adjust the signal trace thickness on the trace line side. A similar design choice needs to be considered between the trace line and the housing, because also there a good match is critical for optimal performance. This means that unless optimization of the RF interfacing already starts at PIC design level, compromises to the RF transmission efficiency may need to be made.

7.11.3 RF signal spacing

If PCBs are used for the redistribution of the electrical signals, these contain ground connected vias between the signal traces to shield them from interferences and avoid signal resonances. The preferred minimum diameter of these vias for many commercial off-the-shelf PCB suppliers is 300 µm. Given our three objectives for RF interfacing, this via diameter, together with the chosen dimensions of the signal and ground traces, dictates the preferred spacing *p* of RF trace lines on your PIC. We recommend a pitch *p* of 600 µm, which is a guideline widely adapted in the industry. This guideline, which considers a pad width on the PCB of 100 µm and a pitch between adjacent pads (both signal and ground) of 200 µm, enables a standard, reliable, and cost-effective PCB manufacturing process. In case the ground connections can be shared between adjacent GSG clusters, a higher density can be achieved. Please involve PHIX in the PIC design to achieve the optimal layout and density of RF ports.

PHIX can perform wire bonding on smaller pad sizes or signal pitches, but this may negatively impact RF performance as, for example, wire bonds would become longer and ribbon wires may be unfit for small bond pads. If a higher density is required, please get in contact with PHIX to ensure that your PIC design can be feasibly packaged with the required RF performance.

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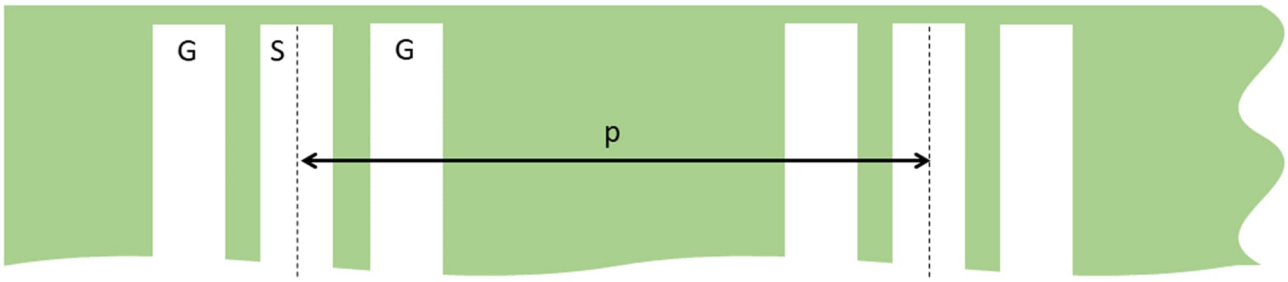

Figure 23: Trace line spacing for single-ended traces

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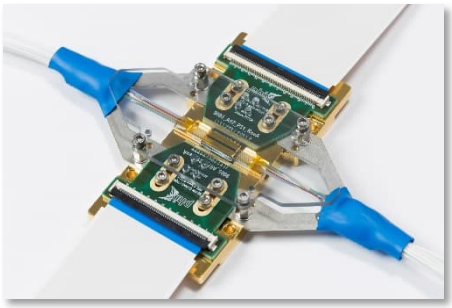
8 Overview of Standard Package Types

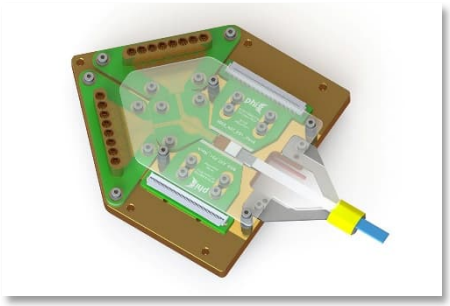
Below is a cross-section of some standard package types offered by PHIX. Each of these have characteristics that favor certain chip dimensions and system configurations. More standard package types, and the features and specifications of each of these, are outlined in a table on the PHIX website.

Besides our selection of standard housings, PHIX can support many other industry standards or customer-specific packages. If you have special requirements, we can even design a customized package for you.

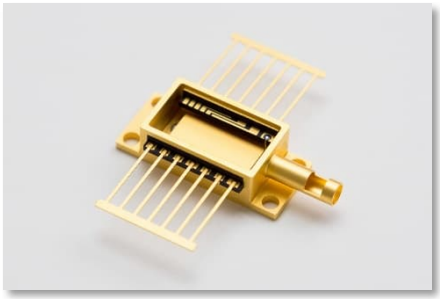
PHIX Characterization Package



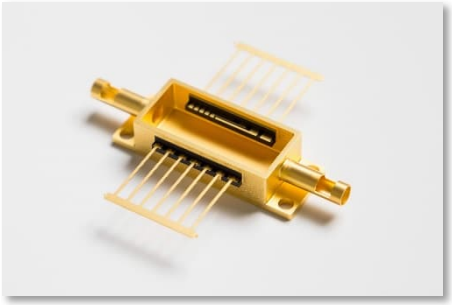
PHIX RF Characterization Package



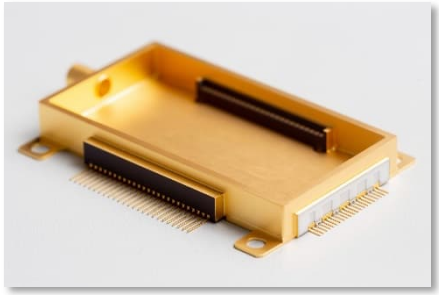
14-pin Butterfly



Dual optical 14-pin Butterfly



Large Area Gold Box



LCP Overmolded Leadframe